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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/398,707 | 09/20/1999 | CHARLES E. POLK JR. | SC10900TS | 1432 |

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FREESCALE SEMICONDUCTOR, INC.
LAW DEPARTMENT
7700 WEST PARMER LANE MD:TX32/PL02
AUSTIN, TX 78729

| EXAMINER | |
|---|---|
| CHAUDRY, MUJTABA M | |
| **ART UNIT** | **PAPER NUMBER** |
| 2133 | |

DATE MAILED: 08/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/398,707 | POLK ET AL. | |
| | Examiner | Art Unit | |
| | Mujtaba K Chaudry | 2133 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *13-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

Applicant's arguments/amendments with respect to amended claims 13 and 20 and original claims 14-19 and 21-26 filed April 20, 2004 have been fully considered. As a result claims 13-26 are hereby rejected in a non-final action under new grounds of rejection.

### *Claim Rejections - 35 USC § 103*

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 13-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Modlin et al (USPN 6480475) further in view of Carmon et al. (USPN 5404522).

As per claim 13, 20 and 24-26, Modlin et al (herein after: Modlin) substantially teaches (title and abstract) a method and apparatus that provides flexibility in setting user data rates and managing delays in data transmission systems using a super-frame structure and Time Division Duplexing (TDD). Modlin teaches insertion of dummy words into a data stream to be transmitted. By inserting the dummy words, the apparatus is able to render codewords, symbols and super-frames independent from user data rates. As a result, a wide range of user data rates

are available in data transmission systems using a super-frame and TDD. Modlin teaches (col. 3, lines 2-33 & figure 1B) a remote receiver 150 which receives analog signals that have been transmitted over a channel by a transmitter. The received analog signals are supplied to an analog-to-digital converter (ADC) 152, which converts the received analog signals to digital signals. The digital signals are then supplied to a Fast Fourier Transform (FFT) unit 154 that demodulates the digital signals while converting the digital signals from a time domain to a frequency domain as stated in the present application. The demodulated digital signals are then supplied to a frequency domain equalizer (FEQ) unit 156, which performs equalization on the digital signals so the attenuation and phase are equalized over the various frequency tones. Then, a data symbol decoder 158 receives the equalized digital signals, which decodes the equalized digital signals to recover the data, or bits of data, transmitted on each of the frequency tones. In decoding the equalized digital signals, the data symbol decoder 158 needs access to the bit allocation information and the energy allocation information that were used to transmit the data. Hence, the data symbol decoder 158 is coupled to a received bit allocation table 162 and a received energy allocation table 160 which respectively stores the bit allocation information and the energy allocation information that were used to transmit the data. The examiner would like to point out the functionality of the first processor in the present application is included within the method and apparatus of Modlin, since the first processor is stated to perform time to frequency conversion, equalization and decoding of the received data. The data obtained from each of the frequency tones is then forwarded to the forward error correction (FEC) unit 164. The FEC unit 164 performs error correction on the data to produce corrected data. The corrected data is then stored in a buffer 166. The examiner would like to point out that the error correction taught by

Modlin takes place in the FEC unit 164, which is analogous to the functionality of the second processor in the present application.

Modlin does not explicitly teach at least one operation performed by the first processor and the second processor to be dynamically reassigned.

However, Carmon et al. (herein after: Carmon), in an analogous art, substantially teaches those limitations lacking in Modlin. Carmon teaches (title and abstract) a system and method for constructing a partitioned queue of DMA data transfer request for movements of data between a host processor and a digital signal processor (DSP). A multi-media user task (host) computer is interfaced to a high speed DSP which provides support functions to the host computer via an interprocessor DMA bus master and controller. Support of multiple dynamic hard real-time signal-processing task requirements are met by posting signal processor support task requests from the host processor through the interprocessor DMA controller to the signal processor and its operating system. The signal processor builds data transfer packet request execution lists in a partitioned queue in its own memory and executes internal signal processor tasks invoked by users at the host system by extracting signal sample data from incoming data packets presented by the interprocessor DMA controller in response to its execution of the DMA packet transfer request queues built by the signal processor in the partitioned queue. Processed signal values etc. are extracted from signal processor memory by the DMA interprocessor controller executing the partitioned packet request lists and delivered to the host processor. A very large number of packet transfers in support of numerous user tasks and implementing a very large number of DMA channels is thus made possible while avoiding the need for arbitration between the channels on the part of the signal processor or the host processor. In particular, Carmon teaches a

signal processor computer system and to direct memory access control; more specifically, it relates to a dynamic, hard real-time, multi-task signal processing demands commonly encountered in multi-media computer systems. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the techniques taught by Carmon, dynamically reassigned at least one operation performed by one processor to the other, with the method and apparatus of Modlin. This modification would have been to one of ordinary skill because one of ordinary skill in the art would have recognized that by dynamically reassigning tasks between the two processors would efficiently support real-time multi-tasking and thus enhance the reliability.

As per claim 14, Modlin substantially teaches, in view of above rejections, (col. 10, lines 38-41) the series of codewords from the FEC unit 310 are supplied to an interleaver unit 312. The interleaver unit 312 rearranges the codewords for better transmission characteristics.

As per claim 15, Modlin substantially teaches, in view of above rejections, (col. 12, lines 35-44) the FEC unit 310 to perform error correction coding in accordance with a code rate (n/k), where n is the codeword size in bits, k is the data-word size in bits, and n – k = r which is a redundancy quantity in bits. The integers n and k are, for example, the Reed Solomon codeword lengths, in bits, after and before encoding respectively. Reed Solomon codes are implemented in terms of bytes so that n and k are multiples of eight.

As per claim 16, Modlin substantially teaches, in view of above rejections, (col. 10, lines 10-22) data to be retrieved from the buffer 304 and supplied to a Cyclic Redundancy Check (CRC) unit 306 as stated in the present application. The CRC unit 306 operates to add additional

bits (referred to as CRC bits) to the data stream. The additional bits added by the CRC unit 306 can include any additional information to be sent over the channel.

As per claims 17-19, 21 and 22, Modlin substantially teaches, in view of above rejections, (col. 1, lines 16—col. 2, lines 1-64) digital data transmission systems are presently being developed for high-speed data communications. One standard for high-speed data communications over twisted-pair phone lines that has developed is known as Asymmetric Digital Subscriber Lines (ADSL). Another standard for high-speed data communications over twisted-pair phone lines is known as Very High Speed Digital Subscriber Lines (VDSL). In general, these high-speed data communications techniques are referred to as xDSL systems. The standardized system defines the use of a discrete multi tone (DMT) system that uses 256 "tones" or "sub-channels" that are each 4.3125 kHz wide in the forward (downstream) direction. The examiner would like to point out that ATM and TCP/IP are inherently included within the apparatus of Modlin, since both protocols may be used in high-speed networks.

As per claim 23, Modlin substantially teaches, in view of above rejections, (col. 3, lines 25-34) a FEC unit 164 that performs error correction on the data to produce corrected data, which is then stored in a buffer 166. Furthermore, Modlin teaches (col. 7, lines 47-67) a buffer that receives and stores a data quantity to be transmitted and a first insertion unit that determines a first quantity of dummy data and inserts the first quantity of dummy data into the data quantity supplied from the buffer to produce an enlarged data quantity. An error correction unit that receives the enlarged data quantity and performs redundancy coding to produce a redundancy data quantity and a data symbol encoder that receives the redundancy data quantity to be transmitted and encodes bits associated with the redundancy data quantity to frequency tones of a

frame. Modlin also teaches a multicarrier modulation unit that modulates the encoded bits on the frequency tones of a frame to produce modulated signals and a digital-to-analog converter that converts the modulated signals to analog signals. Moreover Modlin teaches the apparatus can further include a second insertion unit that determines a second quantity of dummy data and inserts the second quantity of dummy data into the redundancy data quantity supplied from the error correction unit to produce a modified redundancy data quantity.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Modlin teaches a method and apparatus that provides flexibility in setting user data rates and managing delays in data transmission systems using a super-frame structure and Time Division Duplexing (TDD). Carmon teaches a system and method for constructing a partitioned queue of DMA data transfer request for movements of data between a host processor and a digital signal processor (DSP). Applicant is further invited to read/review additional pertinent prior art that have been appended herein.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 703-305-7755. The examiner may normally be reached Mon – Thur 7:30 am to 4:30 pm and every other Fri 8:00 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 703-305-9595. The fax phone number for the organization where this application is assigned is 703-746-7239.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the receptionist at 703-305-3900.

Mujtaba Chaudry
Art Unit 2133
July 13, 2004

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100